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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/781,336

02/17/2004

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EXAMINER

DO, CHAT C

ART UNIT

PAPER NUMBER

2193

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07/23/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/781,336	Applicant(s) SAHA ET AL.	
	Examiner CHAT C. DO	Art Unit 2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 May 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This communication is responsive to Amendment filed 05/23/2008.
2. Claims 1-23 are pending in this application. Claims 1, 5, 9, 16 and 21 are independent claims. This Office Action is made non-final after a RCE filed 05/23/2008.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-23 cite a method and system for performing FFT/IFFT in accordance with a mathematical algorithm. However, claims 9-23 merely disclose series mental steps/components for performing FFT/IFFT without disclosing a practical/physical application. Further, the claims 1-23 appear to preempt every substantial practical application of the idea embodied within the claims by just computing a number of butterfly stages and distributing among processors. Therefore, claims 1-23 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 9-10, 16-17, and 20-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Laxmi et al. (“Performance Analysis of FFT Algorithms on Multiprocessor Systems”).

Re claim 1, Laxmi et al. disclose in pages 512-521 a scalable method for implementing FFT/IFFT computations in multiprocessor architectures (e.g. abstract section in page 512) that provides improved throughput by eliminating the need for inter-processor communication after the computation of the first "log.sub.2P" stages (e.g. first two stage of Figure 2) of the FFT/IFFT computations for a multiprocessor architecture including an implementation using "P" processing elements (e.g. four processing elements in Figure 2), comprising the steps of:

computing each butterfly of the first "log.sub.2P" stages on either a single processing element or on each of the "P" processing elements simultaneously (e.g. Figure 2, wherein $P = N/P$ as seen in section II “Radix-2 FFT computation” in right column page 513, particularly step 1), and

distributing the computation of the butterflies in all the subsequent stages among the "P" processors such that each chain of cascaded butterflies consisting of those butterflies that have inputs and outputs connected together, are processed by the same processor (e.g. Figure 2, section II “Radix-2 FFT computation” in right column page 513, particularly steps 2-3).

Re claim 2, Laxmi et al. further disclose in pages 512-521 the distributing of the computation of the butterflies subsequent to the first "log.sub.2P" butterflies is achieved by assigning operand addresses of each set of butterfly operands to each processor in such a manner that the butterfly is processed by the same processor that computed the connected butterfly of the previous stage in the same chain of butterflies (e.g. Figure 2, section II "Radix-2 FFT computation" in right column page 513, particularly steps 2-3 and first paragraph of right column in page 514).

Re claim 9, it has similar limitations cited in claim 1. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 10, Laxmi et al. further disclose in pages 512-521 the first log.sub.2(P) stages of the transform are calculated on all of the processors operating in parallel (e.g. Figure 2 and first paragraph of right column in page 514).

Re claim 16, Laxmi et al. disclose in pages 512-521 a processor system, comprising: a plurality of processors operable to execute a fast Fourier transform or inverse fast Fourier transform algorithm on a plurality of inputs to generate a plurality of outputs (e.g. PE1-PE4 in Figure 2), each transform including a plurality of stages containing at least one butterfly computational block (e.g. butterfly operation in PE), and the processors operable to the butterfly computational block for the first "log.sub.2P" stages of the transform on either a single one of the processors or on a plurality of the processors operating in parallel (e.g. Figure 2, wherein $P = N/P$ as seen in section II "Radix-2 FFT computation" in right column page 513, particularly step 1); and address circuitry operable to distribute the computation of the butterfly computational blocks in

all stages subsequent to the first log.sub.2P states among the plurality of processors such that each chain of cascaded butterfly computational blocks in the transform are coupled in series and are computed by the same processor (e.g. Figure 2, section II “Radix-2 FFT computation” in right column page 513, particularly steps 2-3).

Re claim 17, it has similar limitations cited in claim 13. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 20, Laxmi et al. further disclose in pages 512-521 each of the processors comprises a digital signal processor (e.g. introduction section in page 512).

Re claim 21, it has similar limitations cited in claim 16. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Re claim 22, Laxmi et al. further disclose in pages 512-521 the electronic system comprises a communications system (e.g. abstract and introduction sections in page 512).

Re claim 23, it has similar limitations cited in claim 20. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 20.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laxmi et al. (“Performance Analysis of FFT Algorithms on Multiprocessor Systems”).

Re claim 11, Laxmi et al. further disclose in pages 512-521 the method is performed on two processors (e.g. last paragraph left column and first paragraph right column in page 514 wherein $P = 2$), and wherein the first two stages of a radix-2 fast Fourier transform or inverse fast Fourier transform are calculated, and wherein the subsequent stages of the transform are computed as radix-2 stages (e.g. Figure 2 as radix-2). Laxmi et al. fail to disclose in pages 512-521 the first two radix-2 can be performed as radix-4. However, the implementation logically and mathematically of radix-4 as two radix-2 or vice versa is well known in the art of technology and widely used. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace the two radix-2 as one radix-4 into Laxmi et al.'s invention because it would enable to increase the system performance by operating the radix-4 in single unit.

Re claim 12, Laxmi et al. further disclose in pages 512-521 chains comprises a single loop that iterates $N/2 * (\log_2(N/2)) / (\text{number of processors})$ times (e.g. Figure 2 and step 3 in the last paragraph right column in page 513).

Re claim 13, Laxmi et al. further disclose in pages 512-521 each butterfly computational block includes a plurality of operands each having an associated address (e.g. fetching data from storage), and wherein calculating chains of butterfly computational blocks corresponding to the subsequent stages comprises assigning addresses to each of the operands so that each butterfly block in a chain is calculated in the same processor (e.g. Figure 2).

Response to Arguments

9. Applicant's arguments filed 05/23/2008 have been fully considered but they are not persuasive.

a. The applicant argues in page 8 fifth paragraph for claims rejected under 35 U.S.C. 101 that the claims are not directed to the FFT/IFFT computations or algorithm but rather to a method of controlling a multiprocessor system to perform such the calculations. Thus, the claims are directed to statutory subject matter and should be patentable.

The examiner respectfully submits that the claims are rejected under 35 U.S.C. 101 for two reasons: without disclosing a practical/physical application and preemption. For claims 9-23, these claims disclose a method and system for performing FFT/IFFT comprising only two steps: the butterfly computation and chain of butterfly computation among processors. Even though, the claims lightly mentions a plurality of processor in computation, but there is no architecture or how the data is distributed among the processors in the multi-cores/processors as alleged by the applicant above. In addition, all the claims, particularly independent claims, are cited so broad that they merely cover two steps butterfly computations and distributing the computations among processors which are seen in almost FFT/IFFT computations in multi-cores/processors. Thus, the claims 1-23 appear to preempt every substantial practical application of the idea embodied within the claims by just computing a number of butterfly stages and distributing among processors. There is nothing in the claims would specifically direct to a method of controlling a multiprocessor system as alleged by the applicant above.

b. The applicant argues in page 9 second paragraph for claim 1 that the primary reference discloses the PE starts to communicate with each other after $\log_2(N/P)$ computations wherein claim 1 discloses the communications among the PEs happens only after $\log_2(P)$ stages and only once for the rest of the FFT computation as evident from Figures 2-3.

The examiner respectfully submits that the alleged limitations “the communications among the PEs happens only after $\log_2(P)$ stages and only once for the rest of the FFT computation” might be seen in Figures 2-3, but not directly seen in the claim 1. Claim 1, based on the claim language, does not disclose any direct communications among the PEs ONLY after $\log_2(P)$ stages and ONLY once for the rest of the FFT computation as mentioned above. Thus, the examiner does not need to address/show this alleged limitations in the primary reference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

July 21, 2008

<i>Application Number</i> 	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/781,336	SAHA ET AL.	
	Examiner	Art Unit	
	CHAT C. DO	2193	